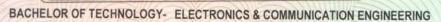


## HYDERABAD - 500 085, ANDHRA PRADESH, INDIA

CONSOLIDATED MARKS MEMO / CREDIT SHEET



0446168

Serial No.:

21101027371

SHAIKH SAMEER KHALIL

Name of the College :

5A-TMITS, INDRESHAM

Month & Year of Final Exam: April, 2014

S.No.	SUBJECT TITLE	INT	EXT	TOTAL	CREDITS	S.No.	SUBJECT TITLE	52 INT MARKS	EXT	TOTAL	- CHICAGO
	Maximum Marks in Theory	25	75	100		S	Maximum Marks in Lab		50	75	
			100	1	YEAR	2					
	DIRECT ADMISSION INT	Γ <b>Ο</b> ΙΙ	I-Y	EΑ	R	U	NDER LATERAL ENTRY	sc	HE	ME	=
1	I SEMESTER				YEA		II SEMESTER				
	MATHEMATICS-III	19	100	54*	-3-	1	PRINCIPLES OF ELECTRICAL ENGINEERING	23	49		1
2	PROBABILITY THEORY & STOCHASTIC PROCESSES	24		55	3	2	ELECTRONIC CIRCUIT ANALYSIS	16	56	ALC: YELL	1
2	ENVIDONMENTAL CTUDIES		1.34	62	3	3	PULSE & DIGITAL CIRCUITS	24	49	73	1
	ENVIRONMENTAL STUDIES	21/20		74			CIMITOLINIO TUEODY A LOGIC DESIGN	E 2			
1	ELECTRIC CIRCUITS	22	52	74	4	4	SWITCHING THEORY & LOGIC DESIGN	24	52		
4	ELECTRIC CIRCUITS ELECTRONIC DEVICES & CIRCUITS	22 22	52 45	67	4	5	ELECTROMAGNETIC THEORY & TRANSMISSION LINES	24 21	37	58	
4 5	ELECTRIC CIRCUITS	22	52 45 43	67 64	4		ELECTROMAGNETIC THEORY & TRANSMISSION LINES ELECTRICAL ENGINEERING LAB	24 21 24	37 49	58 73	
5	ELECTRIC CIRCUITS ELECTRONIC DEVICES & CIRCUITS SIGNALS & SYSTEMS	22 22 21	52 45 43 43	67	4	5	ELECTROMAGNETIC THEORY & TRANSMISSION LINES	24 21	37	58 73 68	
4 5 6 7	ELECTRIC CIRCUITS ELECTRONIC DEVICES & CIRCUITS SIGNALS & SYSTEMS ELECTRONIC DEVICES & CIRCUITS LAB	22 22 21 24	52 45 43 43	67 64 67 66	4 4 2	5 6 7 8	ELECTROMAGNETIC THEORY & TRANSMISSION LINES ELECTRICAL ENGINEERING LAB ELECTRONIC CIRCUIT ANALYSIS LAB	24 21 24 20	37 49 48	58 73 68	
3 4 5 6 7 7 8	ELECTRIC CIRCUITS ELECTRONIC DEVICES & CIRCUITS SIGNALS & SYSTEMS ELECTRONIC DEVICES & CIRCUITS LAB BASIC SIMULATION LAB	22 22 21 24	52 45 43 43	67 64 67 66	4 4 2 2	5 6 7 8	ELECTROMAGNETIC THEORY & TRANSMISSION LINES ELECTRICAL ENGINEERING LAB ELECTRONIC CIRCUIT ANALYSIS LAB PULSE & DIGITAL CIRCUITS LAB	24 21 24 20	37 49 48	58 73 68	
4 5 6 6 7 7 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	ELECTRIC CIRCUITS ELECTRONIC DEVICES & CIRCUITS SIGNALS & SYSTEMS ELECTRONIC DEVICES & CIRCUITS LAB BASIC SIMULATION LAB  I SEMESTER	22 22 21 24 24	52 45 43 43 42	67 64 67 66	4 4 2 2 YEA	5 6 7 8	ELECTROMAGNETIC THEORY & TRANSMISSION LINES ELECTRICAL ENGINEERING LAB ELECTRONIC CIRCUIT ANALYSIS LAB PULSE & DIGITAL CIRCUITS LAB  II SEMESTER	24 21 24 20 23	37 49 48 49	58 73 68 72 68	

	I SEMESTER			IV	YEA	R	II SEMESTER					
8	IC APPLICATIONS (LAB)	24	46	70	2	8	ADVANCED ENGLISH COMMUNICATION SKILLS (LAB)	23	44	67	2	
7	ANALOG COMMUNICATIONS (LAB)	23	43	66	2	7	DIGITAL SIGNAL PROCESSING (LAB)	23	47	70	2	
6	IC APPLICATIONS	22	50	72	3	6	MICROPROCESSORS & MICROCONTROLLERS (LAB)	22	48	70	2	
5	ANALOG COMMUNICATIONS	22	39	61	3	5	DIGITAL SIGNAL PROCESSING	20	50	70	4	
-21	ELECTRONIC MEASUREMENTS & INSTRUMENTATION	23	50	73	4	4	MICROPROCESSORS & MICROCONTROLLERS	23	27	50*	4	
3	ANTENNAS & WAVE PROPAGATION	24	64	88	3	3	DIGITAL COMMUNICATIONS	21	60	81	3	
2	COMPUTER ORGANIZATION	24	41	65	4	2	OPERATING SYSTEMS	21	38	59	4	
1	CONTROL SYSTEMS	24	33	57	4	1	MANAGERIAL ECONOMICS & FINANCIAL ANALYSIS	21	47	68	4	

	I SEMESTER		3	IV	YE	AR	II SEMESTER				
	MANAGEMENT SCIENCE	21	33	54	3	1	CELLULAR & MOBILE COMMUNICATIONS	24	36	60	3
	VLSI DESIGN CONTRACTOR OF THE PROPERTY OF THE	24	49	73	4	2	RADAR SYSTEMS	24	31	55	3
	MICROWAVE ENGINEERING	21	51	72	3	3	WIRELESS COMMUNICATIONS & NETWORKS	24	54	78	3
	COMPUTER NETWORKS	21	40	61	4	4	INDUSTRY ORIENTED MINI PROJECT	2	44	44	2
	DIGITAL IMAGE PROCESSING	24	47	71	3	5	SEMINAR	49		49	2
	EMBEDDED SYSTEMS	23	44	67	4	6	MAJOR PROJECT	49	128	177	1
	E-CAD AND VLSI LAB	24	50	74	2	7	COMPREHENSIVE VIVA		1	95	2
8	MICROWAVE ENGG. AND DIGITAL COMMNS. LAB	23	48	71	2						
			20				(# Project Internal= 50, External=150)				

Number of Credits registered for: 150 Aggregate Marks Secured for best: 143

Aggregate Marks Secured: 3157 OUT OF 4200 (75.17%)

Date of Issue: June 13, 2014

(see overleaf for Rules concerned to award of class) A indicates 'ABSENT

(\*Courses registered but not counted for calculation of aggregate)

CONTROLLER OF EXAMINATIONS